A Monotonic, low power and high resolution digitally controlled oscillator

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Paper Reference Number: ELE-3032

Name of the Presenter: Rashin Asadi

Abstract

In this paper a monotonic and low power Digitally controlled oscillator (DCO) is presented. The proposed DCO uses a cascading structure to achieve high resolution and wide frequency range at the same time. In addition it employs the interpolation method to solve the non monotonic problem in cascading structure. The proposed DCO has been simulated with a standard performance 65nm complementary metal-oxide semiconductor process. Simulation result shows that power consumption can be improved to 114µw (@1.516GHZ), and 81µw (@447.1MHZ) with 0.8 ps resolution.

Key words: Digitally controlled oscillator (DCO), Low power, Monotonic, High resolution, jitter

1. Introduction

Phase locked loop is a very important clocking circuit for many integrated circuits to clock and data recovery or frequency synthesis. Traditionally PLLs such as charge pump-based PLLs are designed by analog approaches. However charge pump-based PLLs suffer from a serious leakage current problem in a 65-nm complementary metal-oxide semiconductor (CMOS) process (Chung, Ko and Shen, 2011). As the technology scales, the supply voltage decreases, and the allowable range of control voltage on VCO decreases as well. Also as the technology scales, VCO's gain increases and oscillators become more sensitive to the supply and substrate noise and the voltage control. In addition, integrating an analog block into a digital system in SOC, takes more design efforts. Furthermore as technology migrates, the analog blocks need to be re-designed.
Recently all digital phase locked loop (ADPLL) which uses digitally controlled oscillator in its structure has been proposed. Since it is operating in digital domain, it is less sensitive to supply and substrate noise. In addition, ADPLLs use digital design approaches so they are suitable to be integrated in SOC. Furthermore, ADPLL which uses robust digital code to control DCOs can avoid leakage current problem (Chung, Ko and Shen, 2011). Fig. 1 indicates an all digital phase locked loop. The time to digital converter (TDC) translates the input timing error to a digital code, and the digital loop filter (DLF) smoothen the error to generate a control signal in the digital form to drive the digitally controlled oscillator (DCO) (Moon, Park and Jeong, 2008). The DCO is the most important block in ADPLL. The DCO is the major source of power consumption and jitter in ADPLL, and its controllable range directly determines the controllable range of ADPLL. Hence, how to design a low power DCO with high frequency resolution and wide frequency range is very important in designing ADPLL systems.

![ADPLL Diagram](image)

**Fig. 1:** The general form of an ADPLL

The simplest DCO that directly uses a ring of inverters, has insufficient resolution for most applications (Olsson and Nilsson, 2003). The current-starved DCO which changes the delay of each stage to determine the output frequency, has a good resolution but high static power consumption (Kumar, Arya and Pandey, 2012). Additionally, such approach demands high complexity at circuit level, resulting in long design cycle and low portability (Sheng, Chung and Lan, 2012). Implementing DCOs with standard cells simplifies the design, when process or specification is changed, and enhances portability to different processes. In order to increase resolution, OR-AND-Inveters (OAI) based DCOs are proposed. However, the linearity remains to be solved (Wu, Wang, Wey and Wu, 2005). Also digitally controlled varactor (DCV) has a good resolution and linearity, but to provide wider frequency range, many DCV cells should be used. hence, its power consumption will be increased (Chen, Chung and Lee, 2005). Cascaded hysteresis delay cells (CHDC) have very little power consumption, but the process, voltage and temperature (PVT) variations of the CHDC delay is high due to some weak driven internal nodes (Hsu, Yu and Lee, 2010). Interlaced hysteresis delay cells (IHDC) prevent the short-circuit current and save the leakage current, so achieve a low power (Yu, Chung, Yu and Lee, 2012). But, its power consumption is still high.

In order to achieve both high resolution and wide frequency range at the same time, the cascading structure has been proposed (Chen, Chung and Lee, 2005), (Sheng, Chung and Lee, 2008), (Erfani Majd, Lotfizad, 2011). It should be noted that in cascading structure, to ensure that there will not be any frequency dead zone larger than the LSB resolution of DCO with process, voltage, and temperature (PVT) variations, the controllable range of each stage must be larger than the delay step of the previous stage. This induces some
overlap regions between subfrequency bands. Because of these overlap regions between subfrequency bands, the non-monotonic problem will occur in the output frequency. As non-monotonic problem causes large delay change, it will increase the phase error and cycle-to-cycle jitter in cascading structure DCOs. Also using the non-monotonic DCO in an ADPLL system may cause DCO to get stuck between two control codes forever, resulting in unlock phenomenon. To overcome the non-monotonic problem, many works have used the interpolation method in their fine tuning stage (Moon, Park and Jeong, 2008), (Seo, Chun, Jun, Kim and Kwon, 2011). By using the interpolation scheme, the output phase is placed between minimum and maximum delay and guarantees monotonicity over the change of coarse tuning control (Moon, Park and Jeong, 2008). However, the short-circuit current of an interpolator is high. So, when it is needed to use more tri-state buffers to cover a wider step of coarse tuning stage, the power consumption greatly increases.

In this brief, a monotonic, low power and wide frequency range DCO with high resolution is presented for SOC applications. The proposed DCO uses a new interpolation method that has less complexity than the previous methods, and also save power more than the previous works.

The rest of this paper is organized as follows. Section II describes the proposed DCO. Section III shows simulation results and section IV concludes the paper.

2. Proposed DCO

Fig. 2 illustrates the architecture of the proposed monotonic and low power digitally controlled oscillator. the proposed DCO consists of two stages, coarse tuning stage and fine tuning stage, that are cascaded to each other, to have high resolution and wide frequency range at the same time. Based on the required frequency, the delay of the coarse tuning stage and fine tuning stage is controlled by coarse tuning codes \(C[15:0]\), \(EN[15:0]\) and fine tuning codes \(F[6:0]\) respectively.

In order to keep the monotonic response, the interpolation method is used in the fine tuning stage. After selection of two adjacent taps of the coarse tuning path, the fine tuning stage interpolates two output lines regarding to the fine tuning control code. The interpolation method guarantees that the output phase is placed between minimum and maximum delay. So, guarantees the monotonicity when fine tuning stage switches between different coarse tuning stages.

Coarse tuning stage

The coarse tuning stage shown in fig. 3 is identical to the coarse tuning stage used in (Olsson and Nilsson, 2003). The coarse tuning stage consists of 16 coarse delay cells (CDC) which are two-input AND gates. The delay of CDCs determines the delay steps of coarse tuning stage. The coarse tuning stage has two outputs, and regarding to code of TDC, different paths are selected through the coarse chain by codes C0-C15. When a higher frequency is required a shorter path is selected, and the rest of CDCs will not be
used. So to reduce the power consumption, these redundant CDCs will be disabled by codes EN0-EN15.

![Diagram](image_url)

**Fig. 2.** The proposed Digitally Controlled Oscillator (DCO)

![Diagram](image_url)

**Fig. 3.** Coarse tuning stage

Fine tuning stage

To improve the resolution of DCO, the fine tuning stage is added to it. In previous works interpolation methods have been used in the fine tuning stage to maintain the monotonicity of DCO, when switching between different steps of coarse tuning stage. However, as the delay range of coarse tuning steps increases, to cover the delay steps of coarse tuning stage, the number of tri-state buffers which are used in the interpolator block increases. So, the short-circuit current of the interpolator greatly increases, resulting in power consumption increase of the DCO. To solve this problem many schemes have been proposed in later works. Two-level controlled interpolation structure (Sheng, Chung and Lan, 2012) and built-in self-calibration circuit (Chung, Ko and Shen, 2011) are some of them. Two-level interpolator has two stages in it's fine tuning stage. The first stage interpolates the delay steps of coarse tuning stage. As the delay resolution of the first stage is not enough, the second stage interpolates the delay steps of the first stage and increases the delay resolution. But the complexity and the power consumption is still too high. Built-in self-calibration circuit needs an extra calibration block to maintain the delay monotonicity. In this paper a novel single-stage interpolator is presented that has less complexity than previous works and therefore has less power consumption. As it is shown in fig. 2, in the proposed DCO the fine tuning stage has two paths and consists of one interpolator. The first path has no delay while the second path has a delay that is equal to the half of the each step of coarse tuning stage. The interpolation part that is indicated in fig. 4, just can cover half of each delay step of coarse tuning stage. If the required delay of DCO is smaller than the half of delay step of coarse tuning stage, first path is selected while if the required delay is larger than the half of delay step of coarse tuning stage the other path is selected. The interpolator consists of two driving groups that are controlled
by the fine tuning control codes (F[5:0]). As it is shown in fig. 4, the driving groups in the interpolator are composed of binary-weighted tri-state inverters (Combes, Diory and Greiner, 1999). The interpolator part can provide 64 different steps. So, the fine tuning stage can provide 128 different steps.

![Interpolator Diagram](image)

**Fig. 4. Interpolator**

### 3. Simulation Results

The proposed DCO has been simulated in the 65 nm PTM CMOS process. Since the delay step of fine tuning stage determines the delay DCO resolution, the proposed DCO can achieve high resolution with 0.8 ps. Controllable delay range and the finest delay step of coarse and fine tuning stage are shown in table 1. Due to the new single stage interpolator, the power consumption can be reduced to 114 µw at 1516MHZ and 81 µw at 447.1 MHZ with 1v supply voltage.

<table>
<thead>
<tr>
<th></th>
<th>Coarse tuning</th>
<th>Fine tuning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range (ps)</td>
<td>1577.5</td>
<td>99.2</td>
</tr>
<tr>
<td>Step (ps)</td>
<td>100</td>
<td>0.8</td>
</tr>
</tbody>
</table>

Table 1: Simulation results of step/range of tuning stage

The 1.516 GHZ output waveform of the proposed DCO is shown in fig. 5.

Fig. 6 shows the jitter performance of the proposed DCO, evaluated at 1.516 GHZ, by monte carlo simulation under VDD=1v and about 0.12 voltage variation. A 1.9 ps time-period Jitter is measured.
Fig. 5. Output waveform (1.516 GHZ)

Fig. 6. Time-period jitter of the proposed DCO in 1.516 GHZ (Monte Carlo analysis)

The Hspice results shown in fig. 7 and 8 indicate that the output frequency has a monotonic response versus control code when it is switching between two halves of the fine tuning stage, and when it is switching between coarse stages, respectively.

Fig. 7. Output period of DCO when its switching between halves of the Fine tuning stage
Fig. 8. Output period of DCO when its switching between different coarse tuning steps

Table 2 lists the comparison results of the proposed DCO with the state-of-the-art DCOs. In comparison to the other works the proposed DCO has the widest frequency range and the highest frequency resolution. While its power consumption is lower than the state-of-the-art DCOs. In addition the proposed DCO has a monotonic response in it's output waveform.

4. Conclusion

In this paper a monotonic, low power and high resolution DCO, in 65nm CMOS technology is presented. The proposed DCO uses cascading structure to have wide operating range and high resolution at the same time. single stage interpolator in DCO's architecture not only can maintain the monotonic response, but also can reduce the total power consumption and circuit complexity as compared with conventional approaches. Simulation results show that the power consumption of the proposed DCO is improved to 81 µw and 114 µw at 477.1 MHZ and 1516 MHZ respectively with 0.8 ps resolution.

<table>
<thead>
<tr>
<th>process</th>
<th>This work</th>
<th>[6]</th>
<th>[1]</th>
<th>[7]</th>
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<tr>
<td>Supply voltage (v)</td>
<td>65nm CMOS</td>
<td>90nm CMOS</td>
<td>65nm CMOS</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>Operation range (MHZ)</td>
<td>447.1 -1516</td>
<td>3.4-163.2</td>
<td>47.8-538.7</td>
<td>180-530</td>
</tr>
<tr>
<td>LSB resolution (ps)</td>
<td>0.8</td>
<td>2.05</td>
<td>17.4</td>
<td>3.5</td>
</tr>
<tr>
<td>RMS jitter</td>
<td>1.9 ps @ 1516 MHZ (0.3%)</td>
<td>49.3 ps (0.02%@5MHZ)</td>
<td>81.1(DCO (@64.49 MHZ)</td>
<td>20.7 ps @480 MHZ (0.99%)</td>
</tr>
<tr>
<td></td>
<td>166 µw(163.2 MHZ)</td>
<td>142 µw(@58.7 MHZ)</td>
<td>466 µw (@480 MHZ)</td>
<td></td>
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<tr>
<td></td>
<td>205 µw(@481.6 MHZ)</td>
<td>357 µw (@200 MHZ)</td>
<td></td>
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<tr>
<td>Power consumption</td>
<td>81 µw(@ 447.1 MHZ)</td>
<td>5.4 µw(3.4 MHZ)</td>
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<td>Monotonicity</td>
<td>yes</td>
<td>No</td>
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Table 2: Performance Summary
References


